In the Claims:

1. (Currently Amended) A method of forming a semiconductor varactor device having improved linearity comprising the steps of:

providing a semiconductor substrate;

forming at least a first and a second differential varactor clement on said semiconductor substrate, the forming of each of said differential varactor elements comprising the steps of forming first, second and third N+ doped regions in [[an]] the same N well, forming a first gate for controlling said first and second N+ doped regions and forming a second gate for controlling said second and third N+ doped regions;

connecting said first, second and third N+ doped regions of said first differential varactor element to receive power having [[a]] the same first voltage; and

connecting said first, second and third N+ doped regions of said second differential varactor element to receive power having [[a]] the same second voltage, said second voltage being different than said first voltage.

2. (Currently Amended) The method of claim 1 further comprising forming a first resistor, having a first terminal and a second terminal in said semiconductor varactor device connected to receive power from a voltage source, and wherein said step of connecting said first, second and third N+ doped regions of said first differential varactor comprises connecting said regions to said voltage source and to said first terminal of said first resistor, and wherein said step of connecting said first, second and third N+ doped regions of said second differential varactor comprises connecting to said second terminal of ~~voltage source through~~ said first resistor so that power from said voltage source received at said second differential varactor passes through said first resister resulting in a voltage drop.

3. (Original) The method of claim 1 wherein said step of forming said first and second gates comprises the step of forming a first N-type gate and forming a second N-type gate.

4. (Original) The method of claim 2 wherein said step of forming a first resistor comprises the step of forming another resistor and said first resistor and wherein said another resistor is connected in series and between said voltage source and said first resistor, wherein said step of connecting said first, second and third N+ doped regions of said first differential varactor element to receive power from said voltage source comprises the step of connecting said regions to said voltage source through said another resistor, and such that said second differential varactor elements receive power from said voltage source through both of said another and said first resistors.

5. (Original) The method of claim 2 wherein said step of forming at least a first and a second differential varactor element comprises the step of forming at least a first, a second and a third differential varactor element, wherein said step of forming a first resistor comprises the step of forming first and second resistors connected in series and further comprising the step of connecting said first, second and third N+ doped regions of said third differential varactor element to receive power from said voltage source through both of said first and second resistors.

6. (Currently Amended) The method of claim 5 wherein said step of forming first and second resistors comprises the step of forming another resistor and said first and second resistors and wherein said another resistor is connected in series between said voltage source and said first and second resistors and wherein said step of connecting said first, second and third N+ doped regions of said first differential varactor element to receive power from said voltage source

comprises the step of connecting said voltage source to said regions [[only]] through said another resistor.

7. (Original) The method of claim 2 wherein said step of forming first and second differential varactor elements comprises the step of forming a plurality of differential varactor elements, wherein said step of forming a first resistor comprises the step of forming a plurality of resistors connected in series such that nodes are defined between adjacent ones of said serially connected plurality of resistors and further comprising the step of connecting said first, second and third N+ doped regions of one each of said plurality of differential varactor elements to one each of said nodes such that said first, second and third N+ doped regions of different ones of said plurality of differential varactor elements are electrically separated by one of said plurality of resistors.

8. (Original) The method of claim 7 wherein said step of forming a plurality of resistors further comprises the step of forming said plurality of resistors and another resistor and connecting said another resistor in series between said voltage source and said serially connected plurality of resistors and wherein said step of connecting said first differential varactor element to receive power from said voltage source comprises the step of connecting said voltage source to said varactor element through said another resistor.

9. (Original) The method of claim 1 further comprising the steps of connecting said first gate of said first and second differential varactor elements together at a first terminal and connecting said second gate of said first and second differential varactor elements together at a second terminal.

10. (Original) The method of claim 5 further comprising the steps of connecting said first gate of said first, second and third differential varactor elements together at a first terminal and connecting said second gate of said first, second and third differential varactor element together at a second terminal.

11. (Original) The method of claim 7 further comprising the steps of connecting said first gate of said plurality of differential varactor elements together at a first terminal and connecting said second gate of said plurality of differential varactor elements together at a second terminal.

12. (Original) The method of claim 9 further comprising connecting said first and second terminals to an oscillator circuit as a voltage controlled capacitor.

13. (Original) The method of claim 11 further comprising connecting said first and second terminals to an oscillator circuit as a voltage controlled capacitor.

14. (Original) The method of claim 1 wherein said forming steps are according to a CMOS process.

15. (Original) The method of claim 9 wherein said first and second gates are N-type gates.

16. (Original) The method of claim 10 wherein said first and second gates are N-type gates.

17. (Original) The method of claim 11 wherein said first and second gates are N-type gates.

18. (Original) The method of claim 1 further comprising the steps of forming another differential varactor element on said semiconductor, said another differential varactor element

comprising first, second and third P+ doped regions in a P well, a first gate for controlling said first and second P+ doped regions and a second gate for controlling said second and third P+ doped regions, and connecting said first, second and third P+ doped regions to receive power from said voltage source.

19. (Original) The method of claim 2 wherein said step of forming a first resistor comprises the step of forming said first resistor from a polysilicon material.

20.-30. (Canceled)

31. (New) A method of forming a semiconductor varactor device having improved linearity comprising the steps of:

providing a semiconductor substrate;

forming at least a first, second, and third differential varactor element on said semiconductor substrate, the forming of each of said differential varactor elements comprising the steps of forming first, second and third N+ doped regions in an N well, forming a first gate for controlling said first and second N+ doped regions and forming a second gate for controlling said second and third N+ doped regions;

forming a first and a second resistor in said substrate connected in series and connected to receive power form a voltage source

connecting said first, second and third N+ doped regions of said first differential varactor element to receive power having a first voltage;

connecting said first, second and third N+ doped regions of said second differential varactor element to said voltage source through said first resistor so as to receive power having a second voltage different than said first voltage; and

connecting said first, second, and third N+ doped regions of said third differential varactor element to said voltage source through both of said first and second resistors so as to receive power having a third voltage.

32. (New) The method of claim 31 wherein said step of forming first and second resistors comprises the step of forming another resistor and said first and second resistors and wherein said another resistor is connected in series between said voltage source and said first and second resistors and wherein said step of connecting said first, second and third N+ doped regions of said first differential varactor element to receive power from said voltage source comprises the step of connecting said voltage source to said regions through said another resistor.

33. (New) The method of claim 31 further comprising the steps of connecting said first gate of said first, second and third differential varactor elements together at a first terminal and connecting said second gate of said first, second and third differential varactor element together at a second terminal.

34. (New) The method of claim 33 wherein said first and second gates are N-type gates.

35. (New) A method of forming a semiconductor varactor device having improved linearity comprising the steps of:

providing a semiconductor substrate;

forming at least a plurality of differential varactor element on said semiconductor substrate, the forming of each of said differential varactor elements comprising the steps of forming first, second and third N+ doped regions in an N well, forming a first gate for controlling said first and second N+ doped regions and forming a second gate for controlling said

second and third N+ doped regions;

forming a plurality of resistors connected to receive power form a voltage source and connected in series such that nodes are defined between adjacent ones of said serially connected plurality of resistors; and

connecting said first, second and third N+ doped regions of each of said plurality of differential varactor elements to one each of said nodes such that said first, second and third N+ doped regions of different ones of said plurality of differential varactor elements are electrically separated by one of said plurality of resistors.

36. (New) The method of claim 35 wherein said step of forming a plurality of resistors further comprises the step of forming said plurality of resistors and another resistor and connecting said another resistor in series between said voltage source and said serially connected plurality of resistors.

37. (New) The method of claim 35 further comprising the steps of connecting said first gate of said plurality of differential varactor elements together at a first terminal and connecting said second gate of said plurality of differential varactor elements together at a second terminal.

38 (New) The method of claim 11 further comprising connecting said first and second terminals to an oscillator circuit as a voltage controlled capacitor.

39. (New) The method of claim 11 wherein said first and second gates are N-type gates.

40. (New) A method of forming a semiconductor varactor device having improved linearity comprising the steps of:

providing a semiconductor substrate;

forming at least a first, second, and third differential varactor element on said semiconductor substrate, the forming of each of said differential varactor elements comprising the steps of forming first, second and third N+ doped regions in the same N well, forming a first gate for controlling said first and second N+ doped regions and forming a second gate for controlling said second and third N+ doped regions;

connecting said first, second and third N+ doped regions of said first differential varactor element together so as to receive power having the same first voltage;

connecting said first, second and third N+ doped regions of said second differential varactor element together so as to receive power having the second voltage, said second voltage being different than said first voltage;

connecting said first, second, and third N+ doped regions of said third differential varactor element together so as to receive power having the same third voltage, said third voltage being different than either of said first and second voltage.